

Prototype to Production

Capabilities and final tolerances are confirmed during DFM review.

[Free DFM Review](#)

FABRICATION TOLERANCES	
Trace / Space	Down to 3 / 3 mil*
Trace Tolerance	Based on design and copper-weight review
Drill to Copper	Controlled by finished hole and annular-ring design
Solder Mask	Clearance and registration based on pad geometry
Copper to Edge	Defined by profile method and copper construction
Controlled Impedance	Typical +/-10%; tighter targets by review

LAMINATION & STACK-UP	
Layer Count	1-32 layers
Board Thickness	Typical +/-10%, subject to stack-up and material
Lamination	Vacuum and sequential lamination
Layer Registration	Controlled by layer count, material and design
Hybrid Builds	Mixed dielectric and FR-4 / RF constructions

DRILL, ROUTE & PROFILE	
Drilling	Mechanical, laser and controlled-depth drilling
Via Structures	Through, blind, buried, stacked, staggered and via-in-pad
Routing	CNC/laser routing, scoring and route-and-retain
Special Features	Countersinks, counterbores, slots and castellations
Profile Options	Complex outlines, plated edges and edge contacts

CORE CAPABILITIES		
• Rigid PCB • HDI & Microvia • Controlled Impedance • Embedded Passives	• Flexible PCB • RF / Microwave • Heavy Copper • Back Drilling	• Rigid-Flex PCB • High-Frequency PCB • Aluminum PCB • Plated Edges
MATERIALS		
Standard	FR-4 and high-Tg laminate systems	
High-Speed / RF	Low-loss, PTFE and hydrocarbon ceramic systems	
Flexible	Polyimide flex materials and coverlay systems	
Thermal	Aluminum and metal-backed substrates	
Copper Weight	Up to 6 oz external / 4 oz internal*	
SURFACE FINISHES & VIA FILL		
Gold Finishes	ENIG, ENEPIG, hard gold and wire-bondable soft gold	
Solder Finishes	Leaded HASL and lead-free HASL	
Other Finishes	Immersion silver and OSP	
Via Fill	Conductive and non-conductive epoxy fill	
Microvia Fill	Copper-plated and filled microvia structures	
INSPECTION & VERIFICATION		
Electrical Test	Flying probe and netlist-based electrical test	
Optical Inspection	AOI for inner and outer layers	
Impedance Test	Coupon measurement and TDR verification	